

Proposal to Bucknell University's Undergraduate Research Program
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Remote Reconfiguration of Xilinx Virtex-II Pro Field-Programmable Gate Array Boards Over a Network

Juliana Su
js084@bucknell.edu

Class of 2009
Box C1773
(570) 577-5045
Bucknell ID: 10065489

Michael S. Thompson (Faculty Mentor)
michael.thompson@bucknell.edu
Department of Electrical Engineering

Signatures:

Juliana Su

Michael S. Thompson

A. Project Description

Background:

A field-programmable gate array (FPGA) is a programmable digital logic chip that can be coded to implement digital circuits. A computer program is used to draw a schematic diagram of a circuit or create a text file describing a circuit, which is then compiled to generate a file that can be downloaded onto the FPGA. FPGAs, generally soldered onto circuit boards for use, allow for rapid and simplified development of digital circuits, which can be constructed, debugged, and reprogrammed without physically manipulating the FPGA.

Computer networking is the branch of engineering that specializes in the communication between computer systems and devices. The ability to connect computers and devices in a network allows for an exchange of data.

Objectives:

The focus of our research is to investigate how to remotely administer code to individual FPGA boards. Traditional methods of reprogramming these devices include directly connecting to a computer using a parallel port or using a removable memory card. Sending the information over a network, however, is a better, more efficient approach. Our goal is to investigate, design, and implement a system that will allow these boards to be programmed remotely over a network.

Methods:

I am currently taking Introduction to Digital Systems (ELEC 245), which teaches the analysis and design of digital systems. The course lab component applies lecture material to designing complex digital systems on programmable logic devices, specifically FPGA boards. Overall, the course will provide useful background knowledge and skills for this research.

The initial stage of research will consist of searching for and reading relevant investigations of the problem. Some study in this area has already been done; reviewing the research and work of others will provide me with some ideas concerning the best way to approach the research problem.

After a thorough literature search and review, I will spend time familiarizing myself with the Xilinx Virtex-II Pro FPGA board and its software. Understanding how to use the equipment properly will require reading reference manuals and documentation.

In addition to spending time learning how to use the FPGA boards, I will also need to devote some time to studying basic networking concepts. For this project, I will need a basic knowledge of networking, as well as a working knowledge of control and communication network applications, in order to be able to control the boards and send configuration data to them.

Next is the design stage, a time-consuming, yet crucial step in the project. A few weeks will be dedicated to designing the system, due to the importance of the design process; having a good design lowers the chances of encountering major problems during implementation, saving much time in the long run. Items that will need to be considered include the network elements which will connect the devices, configuration of the system, and location of the FPGA boards.

After design comes implementation. As with the design, the implementation stage will also occur over the course of a few weeks. This time will be spent on coding and installing programs and configuring portions of the system.

Finally, to ensure that the system is running as intended, the last stage of the project will consist of testing and debugging. A decent amount of time will be dedicated to this last stage to ensure that any necessary changes or improvements can be made.

Timeline:

- Weeks 1-2: Literature search and review
- Weeks 3-4: Learning necessary background knowledge
- Weeks 5-6: System design
- Weeks 7-9: System implementation
- Weeks 10-11: Testing and debugging

Outcomes:

This project will combine several different disciplines, including digital design, networking, and Linux system configuration and administration. It will be a practical lesson in computer network systems and hardware, though it may be an ambitious project to complete in an eleven-week time period. The goal is to have a properly functioning system at the end of the project; however, the main focus is to explore the possibility and design of transmitting code to these boards over a network. Overall, the results from this project will be beneficial and applicable to future research concerning networking and hardware.

B. Research Environment

For the duration of the research project, Professor Thompson and I will be working in close collaboration. We plan to hold one-hour long meetings at least once a week. In addition to these meetings, we may also schedule weekly group meetings with Professor Kundan Nepal, also from the Department of Electrical Engineering. This project is part of a larger collaborative scholarship agenda between Professor Thompson and Professor Nepal, which involves building a reconfigurable network platform for use in both research and teaching.

All research will be conducted on the Bucknell University campus. I will be using Xilinx Virtex-II Pro FPGA boards from the Electrical Engineering Department. I will also be using electrical engineering lab space to work on this project.